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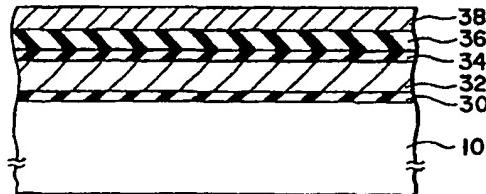
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### ㉚ Mask-ROM manufacturing method.

㉛ A manufacturing method of a mask-ROM of two-layered gate electrode structure is provided. With this method, a cell transistor having a first-layered gate is converted into the depletion type according to data to be stored in the following manner. That is, a first conductive layer (32) is insulatively formed over a semi-conductor substrate (10) of a first conductivity type, a silicon nitride film (36) is formed on the first conductive layer (32), a polysilicon film (38) is formed on the silicon nitride film (36), the polysilicon film (38) is patterned and then altered into a silicon oxide film (46) so as to increase its volume, and the silicon nitride film (36) is patterned with the silicon oxide film (46) used as a mask to form windows (48) for permitting impurity to be doped therethrough. Then, impurity (54) for converting cell transistors into the depletion type according to data to be stored is doped from the windows (48) into the substrate (10) through the first conductive layer (32).



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FIG. 6A

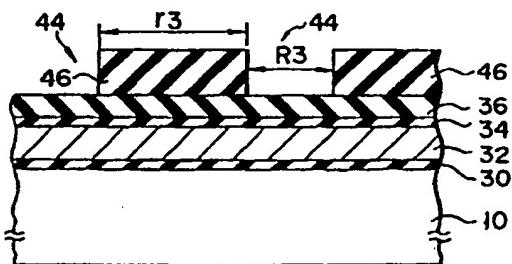


FIG. 6D

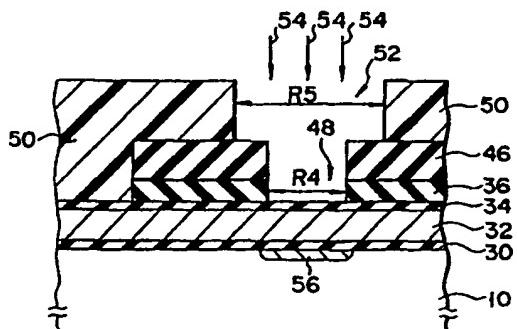


FIG. 6F

## MASK-ROM MANUFACTURING METHOD

This invention relates to a mask-ROM manufacturing method, and more particularly to the improvement of a ROM-Implantation step for storing data.

Conventionally, a mask-ROM is well known as one of nonvolatile semiconductor memory devices. The mask-ROM is a memory in which data can be stored by, for example, selectively ion-implanting impurity into the channel region of memory cell transistors using a mask alignment technique in the manufacturing process so as to selectively form depletion type cell transistors. For example, the mask-ROM constitutes a logic circuit such as an NAND circuit or NOR circuit according to data stored therein.

Fig. 1 is a cross sectional view of a cell of a NAND type mask-ROM. The memory structure of the mask-ROM shown in Fig. 1 is called a two-layered gate electrode structure using two-layered polysilicon gates.

As shown in Fig. 1, a field oxide film 102 is formed in the surface area of a p-type silicon substrate 100 for element isolation, for example. In the isolated element region, n-type source/drain diffusion layers 104A and 104B are formed. The diffusion layer 104A is electrically coupled to a low potential (GND/VSS), for example, and the diffusion layer 104B functions as a bit line and is electrically coupled to a high potential (VDD), for example. First-layered polysilicon gates 108A to 108N and second-layered polysilicon gates 110A to 110C are formed over that portion of the substrate area which lies between the diffusion layers 104A and 104B with a gate oxide film 106 disposed therebetween. The first-layered polysilicon gates 108A to 108N and second-layered polysilicon gates 110A to 110C serve as word lines WL1 to WL<sub>n</sub>. In the channel region below the first-layered polysilicon gates 108A to 108N, n-type diffusion layers 112 (which are hereinafter referred to as short regions) are selectively formed by ion-implantation to selectively convert the cell transistors into the depletion type. Likewise, in the channel region below the second-layered polysilicon gates 110A to 110C, n-type diffusion layers 114 (which are referred to as short regions) are selectively formed by ion-implantation to selectively convert the cell transistors into the depletion type.

The ion-implantation step for selectively converting the cell transistors into the depletion type is generally called a ROM-Implantation step, and in this specification, it is referred to as a ROM-Implantation step or simply a ROM-Implantation.

Now, the integration density of the semiconductor device and semiconductor memory device

is further enhanced and the size of the transistors and the like tends to become smaller. As a matter of course, the integration density in the mask-ROM is significantly enhanced and it is strongly required to reduce the size of the cell transistors.

With the cell structure of two-layered gate electrode type shown in Fig. 1, a distance between the gates (word lines) can be reduced and it is preferable to enhance the integration density of the cell transistors since the second-layered gates 110A to 110C are formed between the first-layered gates 108A to 108N.

However, particularly when a short region 112 for converting the cell transistor having the first-layered gates 108A to 108N into the depletion type is formed, a problem of preventing the high integration density which is explained below occurs.

That is, since the short region 112 is formed below the first-layered gates 108A to 108N, the ROM-Implantation for forming the short region 112 must be effected before the first-layered gates 108A to 108N are formed.

Therefore, it becomes necessary to form the short region 112 larger than necessary so as to have a sufficiently large mask alignment margin so that the first-layered gates can be formed over the short region without fail.

Fig. 2 is a view for explaining an obstacle to enhancement of the integration density and shows an enlarged portion including the first- and second-layered gates.

As shown in Fig. 2, the length of the short region 112 in the gate length direction is equal to the sum of the gate length L1 of the first-layered gate 108 and the mask alignment margins M1 provided on both sides thereof. The mask alignment margin must be approximately 20-30% of the minimum lithography dimensions according to the present lithography technology (in the case of Fig. 2, the gate length L1 of the first-layered gate 108). If the object to be aligned is a diffusion layer such as the short region 112, the mask alignment margin M1 shown in the drawing is set to be 40 to 50% (which range is larger than 20-30%), since due to process fluctuation, the region may expand by the diffusion of impurities and the dimensions of the resist pattern used as a mask may be different from the intended dimensions.

As shown in Fig. 2, in the mask-ROM, the short regions 112 may be formed adjacent to each other depending on data to be stored. Therefore, it becomes necessary to separate the short regions from each other by a certain distance in order to prevent the depletion layers occurring around the short regions 112 from being made in contact with

each other. The distance to be separated is set to  $l_1$  as shown in Fig. 2.

As is understood from the above description, a distance  $l_2$  between the first-layered gates 108 can be so set that  $l_2 = l_1 + 2M_1$ . Further, assuming that an insulation film 116 between the first-layered gate 108 and second-layered gate 110 is made sufficiently thin, then,  $l_2$  becomes substantially equal to the length  $L_2$  of the second-layered gate 110. That is, in the cell structure of second-layered gate electrode type,  $L_1 \ll L_2$ .

The explanation is made more concretely by using actual values.

$L_1$  is set to 0.7  $\mu\text{m}$  and  $l_1$  is set to 0.5  $\mu\text{m}$ . The substantial mask alignment margin  $M_1$  is set to approx. 40% of  $L_1$ , that is, approx. 0.3  $\mu\text{m}$ .

Therefore, the distance  $l_2$  between the first-layered gates is approx. 1.1  $\mu\text{m}$ . Further, if  $l_2$  is substantially equal to  $L_2$ ,  $L_2$  becomes longer than  $L_1$  by more than 50 %.

Thus, in the mask-ROM having the cell structure of two-layered gate electrode type, the distance  $l_2$  between the first-layered gates becomes larger because of its manufacturing method, thereby making it difficult to enhance the integration density.

An object of this invention is to provide a mask-ROM manufacturing method capable of attaining higher integration density.

A mask-ROM manufacturing method comprising: a step (a) of insulatively forming a first conductive layer on a semiconductor substrate of a first conductivity type; a step (b) of forming a first material film which is inactive on said first conductive layer; a step (c) of forming a second material film which is active on said first material film; a step (d) of patterning said second material film; a step (e) of increasing the volume of said second material film by altering the material of said second material film patterned; a step (f) of patterning said first material film with said second material film having an increased volume as a mask and forming windows for doping first impurity in said first material film; a step (g) of selectively doping impurity of a second conductivity type from said first impurity doping window into said substrate through said first conductive layer; a step (h) of selectively altering the material of the surface of said first conductive layer with said patterned first material film used as a mask to selectively form a material altered region on the surface of said first conductive layer; a step (i) of patterning said first conductive layer with said material altered region used as a mask to form first-layered gates and form second impurity doping windows in said first conductive layer; a step (j) of selectively doping impurity of the second conductivity type from said second impurity doping window into said substrate; a step (k) of

insulatively forming a second conductive layer over said first conductive layer and substrate; and a step (l) of patterning said second conductive layer to form second-layered gates.

- 5 According to the mask-ROM manufacturing method having the above steps, the first impurity doping window is formed by patterning the first material film with the second material film whose volume is increased in the step (f) used as a mask.
- 10 Then, impurity of the second conductivity type, that is, impurity for converting the cell transistor into the depletion type is doped from the first impurity doping window into the substrate through the first conductive layer. After this, the material of the surface of the first conductive layer is selectively altered with the first material film which is patterned in the step (h) used as a mask to form the material altered region on the surface of the first conductive layer, and then the first conductive layer is patterned with the material altered region used as a mask to form first-layered gates in the step (i).

As described above, formation of the material altered region used as a mask for patterning the first-layered gate and the doping of Impurity for converting the cell transistor having the first-layered gate into the depletion type can be effected by using the first material film having the same pattern as a mask. Therefore, the short region which lies below the first-layered gate and is used for converting the cell transistor into the depletion type can be formed without providing a mask alignment margin for the first-layered gate.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

- Fig. 1 is a cross sectional view of a cell of a NAND type mask-ROM of two-layered gate electrode structure;
- 40 Fig. 2 is a view for explaining an obstruct to enhancement in the integration density of the conventional mask-ROM;
- 45 Fig. 3 is a plan view of a cell of a NAND type mask-ROM manufactured by a manufacturing method according to one embodiment of this invention;
- 50 Fig. 4 is a cross sectional view taken along the line 4-4 in Fig. 3;
- 55 Fig. 5 is an enlarged view of a portion including first- and second-layered gates of a mask-ROM manufactured by a manufacturing method according to one embodiment of this invention;
- Figs. 6A to 6P are cross sectional views showing enlarged portions each including the first- and second-layered gates of the mask-ROM shown in Fig. 4 in an order of the manufacturing process;
- Fig. 7A is a cross sectional view showing a case

wherein a photoresist is formed in deviated position in a step shown in Fig. 60;

Fig. 7B is a cross sectional view of a structure obtained after an etching process is effected for the structure of Fig. 7A;

Fig. 8A is a cross sectional view showing a first modification of the embodiment of this invention and corresponding to Fig. 6M;

Fig. 8B is a cross sectional view showing a first modification of the embodiment of this invention and corresponding to Fig. 7M; and

Fig. 9 is a cross sectional view showing a second modification of the embodiment of this invention and corresponding to Fig. 4.

There will now be described an embodiment of this invention with reference to the accompanying drawings.

Fig. 3 is a plan view of a cell of a NAND type mask-ROM manufactured by a manufacturing method according to one embodiment of this invention and Fig. 4 is a cross sectional view taken along the line 4-4 of Fig. 3.

As shown in Figs. 3 and 4, the cell structure of a mask-ROM manufactured by a manufacturing method according to one embodiment of this invention basically corresponds to the cell structure of two-layered gate electrode type. For example, a field oxide film 12 is formed in the surface area of a p-type silicon substrate 10 for element isolation. In the isolated element region, n-type source/drain diffusion layers 14A and 14B are formed. The diffusion layer 14A is electrically coupled to a low potential (GND/VSS), for example, and the diffusion layer 14B functions as a bit line and is electrically coupled to a high potential (VDD), for example. First-layered polysilicon gates 18A to 18N and second-layered polysilicon gates 20A to 20C are formed over that portion of the substrate area which lies between the diffusion layers 104A and 104B with a gate oxide film 16 disposed therebetween. The first-layered polysilicon gates 18A to 18N and second-layered polysilicon gates 20A to 20C serve as word lines WL<sub>1</sub> to WL<sub>n</sub>. In the channel region below the first-layered polysilicon gates 18A to 18N, n-type short regions 22 are selectively formed by ion-implantation to selectively convert some of the cell transistors into the depletion type. Likewise, in the channel region below the second-layered polysilicon gates 20A to 20C, n-type short regions 24 are selectively formed by ion-implantation to selectively convert some of the cell transistors into the depletion type.

Fig. 5 is a diagram showing an enlarged portion including the first- and second-layered gates of a mask-ROM manufactured by a manufacturing method according to one embodiment of this invention.

As shown in Fig. 5, the length of the short

region 22 in the gate length direction is equal to the sum of the gate length L1 of the first-layered gate 18 and the extensions D1 due to diffusion of the short region 22 in the right and left directions.

5 The extensions due to the diffusion is approx. 0.1 μm. A distance l1 is so set as to prevent the depletion layers occurring around the short regions l2 from being made in contact with each other.

A distance l2 between the first-layered gates 18 is so set that l2 = l1 + 2D1. Further, an insulation film 26 between the first-layered gate 18 and second-layered gate 20 can be made sufficiently thin in the manufacturing method according to the embodiment of this invention, and l2 becomes substantially equal to the length L2 of the second-layered gate 20.

10 The explanation is made more concretely by using actual values.

l1 is set to 0.7 μm and l1 is set to 0.5 μm. Assume that the extension of diffusion D1 is 0.1 μm.

15 Therefore, the distance l2 between the first-layered gates is approx. 0.7 μm. Further, since l2 is substantially equal to L2, L2 becomes approximately equal to l1.

20 Next, a method for manufacturing the mask-ROM according to one embodiment of this invention is explained with reference to Figs. 6A to 6P.

Figs. 6A to 6P are cross sectional views showing enlarged portions each including the first- and second-layered gates of the mask-ROM shown in Fig. 4 in an order of the manufacturing process.

25 First, as shown in Fig. 6A, a field oxide film (not shown, but in Fig. 4, it is denoted by a reference numeral 12) is formed on a p-type silicon substrate 10. Then, a first silicon oxide film 30 which is used to form a gate insulation film of the first-layered gate is formed to a thickness of approx. 150 Å on the surface of the isolated element region by a thermal oxidation method, for example.

30 After this, a first polysilicon film 32 which is used to form first-layered gates is formed to a thickness of approx. 4000 Å on the entire surface of the semiconductor structure by a CVD method, for example. Next, phosphorus is diffused into the first polysilicon film 32 by using POCl<sub>3</sub>, for example, to make the same conductive (n-type). Then, a sec-

35 ond silicon oxide film 34 is formed to a thickness of approx. 200 Å on the exposed surface of the polysilicon film 32 by a thermal oxidation method, for example. After this, a silicon nitride film 36 is formed to a thickness of approx. 1500 Å on the entire surface of the semiconductor structure by a CVD method, for example. In this case, the second oxide film 34 formed between the silicon nitride film 36 and the polysilicon film 32 is used as a pad film for making it easy to separate the silicon nitride film 36 from the polysilicon film 32. Next,

40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300 305 310 315 320 325 330 335 340 345 350 355 360 365 370 375 380 385 390 395 400 405 410 415 420 425 430 435 440 445 450 455 460 465 470 475 480 485 490 495 500 505 510 515 520 525 530 535 540 545 550 555 560 565 570 575 580 585 590 595 600 605 610 615 620 625 630 635 640 645 650 655 660 665 670 675 680 685 690 695 700 705 710 715 720 725 730 735 740 745 750 755 760 765 770 775 780 785 790 795 800 805 810 815 820 825 830 835 840 845 850 855 860 865 870 875 880 885 890 895 900 905 910 915 920 925 930 935 940 945 950 955 960 965 970 975 980 985 990 995 1000 1005 1010 1015 1020 1025 1030 1035 1040 1045 1050 1055 1060 1065 1070 1075 1080 1085 1090 1095 1100 1105 1110 1115 1120 1125 1130 1135 1140 1145 1150 1155 1160 1165 1170 1175 1180 1185 1190 1195 1200 1205 1210 1215 1220 1225 1230 1235 1240 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2245 2250 2255 2260 2265 2270 2275 2280 2285 2290 2295 2300 2305 2310 2315 2320 2325 2330 2335 2340 2345 2350 2355 2360 2365 2370 2375 2380 2385 2390 2395 2400 2405 2410 2415 2420 2425 2430 2435 2440 2445 2450 2455 2460 2465 2470 2475 2480 2485 2490 2495 2500 2505 2510 2515 2520 2525 2530 2535 2540 2545 2550 2555 2560 2565 2570 2575 2580 2585 2590 2595 2600 2605 2610 2615 2620 2625 2630 2635 2640 2645 2650 2655 2660 2665 2670 2675 2680 2685 2690 2695 2700 2705 2710 2715 2720 2725 2730 2735 2740 2745 2750 2755 2760 2765 2770 2775 2780 2785 2790 2795 2800 2805 2810 2815 2820 2825 2830 2835 2840 2845 2850 2855 2860 2865 2870 2875 2880 2885 2890 2895 2900 2905 2910 2915 2920 2925 2930 2935 2940 2945 2950 2955 2960 2965 2970 2975 2980 2985 2990 2995 3000 3005 3010 3015 3020 3025 3030 3035 3040 3045 3050 3055 3060 3065 3070 3075 3080 3085 3090 3095 3100 3105 3110 3115 3120 3125 3130 3135 3140 3145 3150 3155 3160 3165 3170 3175 3180 3185 3190 3195 3200 3205 3210 3215 3220 3225 3230 3235 3240 3245 3250 3255 3260 3265 3270 3275 3280 3285 3290 3295 3300 3305 3310 3315 3320 3325 3330 3335 3340 3345 3350 3355 3360 3365 3370 3375 3380 3385 3390 3395 3400 3405 3410 3415 3420 3425 3430 3435 3440 3445 3450 3455 3460 3465 3470 3475 3480 3485 3490 3495 3500 3505 3510 3515 3520 3525 3530 3535 3540 3545 3550 3555 3560 3565 3570 3575 3580 3585 3590 3595 3600 3605 3610 3615 3620 3625 3630 3635 3640 3645 3650 3655 3660 3665 3670 3675 3680 3685 3690 3695 3700 3705 3710 3715 3720 3725 3730 3735 3740 3745 3750 3755 3760 3765 3770 3775 3780 3785 3790 3795 3800 3805 3810 3815 3820 3825 3830 3835 3840 3845 3850 3855 3860 3865 3870 3875 3880 3885 3890 3895 3900 3905 3910 3915 3920 3925 3930 3935 3940 3945 3950 3955 3960 3965 3970 3975 3980 3985 3990 3995 4000 4005 4010 4015 4020 4025 4030 4035 4040 4045 4050 4055 4060 4065 4070 4075 4080 4085 4090 4095 4100 4105 4110 4115 4120 4125 4130 4135 4140 4145 4150 4155 4160 4165 4170 4175 4180 4185 4190 4195 4200 4205 4210 4215 4220 4225 4230 4235 4240 4245 4250 4255 4260 4265 4270 4275 4280 4285 4290 4295 4300 4305 4310 4315 4320 4325 4330 4335 4340 4345 4350 4355 4360 4365 4370 4375 4380 4385 4390 4395 4400 4405 4410 4415 4420 4425 4430 4435 4440 4445 4450 4455 4460 4465 4470 4475 4480 4485 4490 4495 4500 4505 4510 4515 4520 4525 4530 4535 4540 4545 4550 4555 4560 4565 4570 4575 4580 4585 4590 4595 4600 4605 4610 4615 4620 4625 4630 4635 4640 4645 4650 4655 4660 4665 4670 4675 4680 4685 4690 4695 4700 4705 4710 4715 4720 4725 4730 4735 4740 4745 4750 4755 4760 4765 4770 4775 4780 4785 4790 4795 4800 4805 4810 4815 4820 4825 4830 4835 4840 4845 4850 4855 4860 4865 4870 4875 4880 4885 4890 4895 4900 4905 4910 4915 4920 4925 4930 4935 4940 4945 4950 4955 4960 4965 4970 4975 4980 4985 4990 4995 5000 5005 5010 5015 5020 5025 5030 5035 5040 5045 5050 5055 5060 5065 5070 5075 5080 5085 5090 5095 5100 5105 5110 5115 5120 5125 5130 5135 5140 5145 5150 5155 5160 5165 5170 5175 5180 5185 5190 5195 5200 5205 5210 5215 5220 5225 5230 5235 5240 5245 5250 5255 5260 5265 5270 5275 5280 5285 5290 5295 5300 5305 5310 5315 5320 5325 5330 5335 5340 5345 5350 5355 5360 5365 5370 5375 5380 5385 5390 5395 5400 5405 5410 5415 5420 5425 5430 5435 5440 5445 5450 5455 5460 5465 5470 5475 5480 5485 5490 5495 5500 5505 5510 5515 5520 5525 5530 5535 5540 5545 5550 5555 5560 5565 5570 5575 5580 5585 5590 5595 5600 5605 5610 5615 5620 5625 5630 5635 5640 5645 5650 5655 5660 5665 5670 5675 5680 5685 5690 5695 5700 5705 5710 5715 5720 5725 5730 5735 5740 5745 5750 5755 5760 5765 5770 5775 5780 5785 5790 5795 5800 5805 5810 5815 5820 5825 5830 5835 5840 5845 5850 5855 5860 5865 5870 5875 5880 5885 5890 5895 5900 5905 5910 5915 5920 5925 5930 5935 5940 5945 5950 5955 5960 5965 5970 5975 5980 5985 5990 5995 6000 6005 6010 6015 6020 6025 6030 6035 6040 6045 6050 6055 6060 6065 6070 6075 6080 6085 6090 6095 6100 6105 6110 6115 6120 6125 6130 6135 6140 6145 6150 6155 6160 6165 6170 6175 6180 6185 6190 6195 6200 6205 6210 6215 6220 6225 6230 6235 6240 6245 6250 6255 6260 6265 6270 6275 6280 6285 6290 6295 6300 6305 6310 6315 6320 6325 6330 6335 6340 6345 6350 6355 6360 6365 6370 6375 6380 6385 6390 6395 6400 6405 6410 6415 6420 6425 6430 6435 6440 6445 6450 6455 6460 6465 6470 6475 6480 6485 6490 6495 6500 6505 6510 6515 6520 6525 6530 6535 6540 6545 6550 6555 6560 6565 6570 6575 6580 6585 6590 6595 6600 6605 6610 6615 6620 6625 6630 6635 6640 6645 6650 6655 6660 6665 6670 6675 6680 6685 6690 6695 6700 6705 6710 6715 6720 6725 6730 6735 6740 6745 6750 6755 6760 6765 6770 6775 6780 6785 6790 6795 6800 6805 6810 6815 6820 6825 6830 6835 6840 6845 6850 6855 6860 6865 6870 6875 6880 6885 6890 6895 6900 6905 6910 6915 6920 6925 6930 6935 6940 6945 6950 6955 6960 6965 6970 6975 6980 6985 6990 6995 7000 7005 7010 7015 7020 7025 7030 7035 7040 7045 7050 7055 7060 7065 7070 7075 7080 7085 7090 7095 7100 7105 7110 7115 7120 7125 7130 7135 7140 7145 7150 7155 7160 7165 7170 7175 7180 7185 7190 7195 7200 7205 7210 7215 7220 7225 7230 7235 7240 7245 7250 7255 7260 7265 7270 7275 7280 7285 7290 7295 7300 7305 7310 7315 7320 7325 7330 7335 7340 7345 7350 7355 7360 7365 7370 7375 7380 7385 7390 7395 7400 7405 7410 7415 7420 7425 7430 7435 7440 7445 7450 7455 7460 7465 7470 7475 7480 7485 7490 7495 7500 7505 7510 7515 7520 7525 7530 7535 7540 7545 7550 7555 7560 7565 7570 7575 7580 7585 7590 7595 7600 7605 7610 7615 7620 7625 7630 7635 7640 7645 7650 7655 7660 7665 7670 7675 7680 7685 7690 7695 7700 7705 7710 7715 7720 7725 7730 7735 7740 7745 7750 7755 7760 7765 7770 7775 7780 7785 7790 7795 7800 7805 7810 7815 7820 7825 7830 7835 7840 7845 7850 7855 7860 7865 7870 7875 7880 7885 7890 7895 7900 7905 7910 7915 7920 7925 7930 7935 7940 7945 7950 7955 7960 7965 7970 7975 7980 7985 7990 7995 8000 8005 8010 8015 8020 8025 8030 8035 8040 8045 8050 8055 8060 8065 8070 8075 8080 8085 8090 8095 8100 8105 8110 8115 8120 8125 8130 8135 8140 8145 8150 8155 8160 8165 8170 8175 8180 8185 8190 8195 8200 8205 8210 8215 8220 8225 8230 8235 8240 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9245 9250 9255 9260 9265 9270 9275 9280 9285 9290 9295 9300 9305 9310 9315 9320 9325 9330 9335 9340 9345 9350 9355 9360 9365 9370 9375 9380 9385 9390 9395 9400 9405 9410 9415 9420 9425 9430 9435 944

second polysilicon film 38 is formed to a thickness of approx. 2000 Å on the entire surface of the semiconductor structure by a CVD method, for example.

After this, as shown in Fig. 6B, a photoresist 40 is formed by coating on the entire surface of the semiconductor structure and openings 42 are formed in the photoresist 40 by a photo etching technique. The openings 42 correspond in position to the first-layered gates to be formed. The opening size R1 of the opening 42 may be the minimum size which can be obtained by the photo etching technique. Likewise, the pattern size r1 of the photoresist 40 may be the minimum size which can be obtained by the photo etching technique.

Then, as shown in Fig. 6C, the polysilicon film 38 is selectively etched by an RIE method, for example, with the photoresist 40 used as a mask to form openings 44 having an opening size R2. After this, the photoresist 40 is removed.

At this time, the pattern size r2 of the polysilicon film 38 is so set as to be approximately equal to r1. Further, the opening size R2 of the opening 44 is approximately equal to R1.

Next, as shown in Fig. 6D, the polysilicon film 38 lying on the silicon nitride film 36 is selectively and thermally oxidized with the silicon nitride film 36 used as an oxidation barrier to alter the same into a silicon oxide film 46. When the polysilicon film 38 is altered into the silicon oxide film 46, the volume of the polysilicon film 38 is increased. As a result, the pattern size r3 of the silicon oxide film 46 becomes larger than r2 and the opening size R3 of the opening 44 becomes smaller than R1.

Then, as shown in Fig. 6E, the silicon nitride film 36 is selectively etched by an RIE method, for example, with the silicon oxide film 46 used as a mask to form openings 48 having an opening size R4. The opening 48 is used as an impurity ion-implanting window for forming a short region below the first-layered gate.

Next, as shown in Fig. 6F, a photoresist 50 is coated on the entire surface of the semiconductor structure and openings 52 are formed in the photoresist by a photo etching technique. The opening 52 is selectively formed according to data to be stored. That is, the opening 52 is formed in position in which a cell transistor having the first-layered gate and converted into the depletion type is to be formed. Since the ion-implantation window (opening 48) is already formed, the opening 52 may be formed simply to expose the window used for the ion-implantation. That is, the photoresist 50 may be formed to cover the window (opening 48) which is not used for the ion-implantation and the opening size R5 of the opening 52 may be set to be larger than the opening size R4 of the opening 48. Then, Phosphorus ions 54 which

are n-type impurity, for example, are ion-implanted into the p-type substrate 10 through the polysilicon film 32 and the like with the photoresist 50 and the like used as a mask (first ROM-Implantation).

In the drawing, a reference numeral 56 denotes a doped region of the substrate 10 into which phosphorus ions 54 are doped.

Then, as shown in Fig. 6G, the photoresist 50 and silicon oxide film 46 are removed.

Next, as shown in Fig. 6H, the exposed surface of the polysilicon film 32 is selectively and thermally oxidized to form a silicon oxide film 58 to a thickness of approx. 1000 Å with the silicon nitride film 36 used as an oxidation barrier.

After this, as shown in Fig. 6I, the silicon nitride film 58 and silicon oxide film 34 are removed.

Then, as shown in Fig. 6J, the polysilicon film 32 is selectively etched by an RIE method, for example, to form a pattern of the first-layered gates 18 with the silicon oxide film 58 used as a mask. An opening 60 having the gate-to-gate size R6 is formed between the first-layered gates 18. The gate-to-gate size R6 becomes approximately equal to dimension r2 of the silicon nitride film 36 (dimension r2 is smaller than dimension r3 of the silicon oxide film 46) since the bird's beak 62 extends as a result of the step shown in Fig. 6H.

Next, as shown in Fig. 6K, a photoresist 64 is formed by coating on the entire surface of the semiconductor structure and openings 66 are formed in the photoresist 64 by a photo etching technique. Like the opening 52 shown in Fig. 6F, the opening 66 is selectively formed according to data stored. The opening 66 is formed in position corresponding to a cell transistor which has a second-layered gate and is converted into the depletion type. Since the ion-implantation window (opening 60) is already formed, the opening 66 may be formed simply to expose the window used for ion-implantation. That is, the photoresist 64 may be formed only to cover or close the window (opening 60) which is not used for ion-implantation and the opening size R7 of the opening 66 may be set to be larger than the opening size R6 of the opening 60. Then, arsenic ions 68 which are n-type impurity, for example, are ion-implanted into the p-type substrate 10 with the photoresist 64 and the like used as a mask (second ROM-Implantation).

In the drawing, a reference numeral 70 denotes a doped region of the substrate 10 into which arsenic ions 68 are doped.

Then, as shown in Fig. 6L, the photoresist 64 is removed.

Next, as shown in Fig. 6M, the silicon oxide film 58 and silicon oxide film 30 are removed. At this time, the silicon oxide film 30 is removed with the first-layered gate 18 used as a mask. As a result, that portion of the silicon oxide film 30 which

lies directly under the first-layered gate 18 is left behind and is used as the gate oxide film 16.

Subsequently, as shown in Fig. 6N, a silicon oxide film 72 is formed on the exposed portions of the substrate 10 and on the first-layered gate 18 by a thermal oxidation method, for example. This thermal oxidation is carried out such that the silicon oxide film 72 formed on the exposed substrate portions has a thickness of approximately 150 Å. Since the silicon oxide film formed on the surface of the substrate 10 will be used as the gate oxide film of the second-layered gate, a reference numeral 16 is attached to the same in the drawing. Then, a third polysilicon film 74 which is used to form the second-layered gate is formed to a thickness of approx. 4000 Å on the entire surface of the semiconductor structure by a CVD method, for example. After this, phosphorus is diffused into the third polysilicon film 72 by using  $\text{POCl}_3$ , for example, to make the same conductive (n-type).

Then, as shown in Fig. 6O, a photoresist 76 is formed by coating on the entire surface of the semiconductor structure and openings 78 are formed in the photoresist 76 by a photo etching technique. The pattern of the photoresist 76 having the openings 78 formed therein corresponds to a pattern for forming the second-layered gate. The opening size R7 of the opening 78 may be the minimum size which can be obtained by the photo etching technique. Likewise, the pattern size r4 of the photoresist 76 may be the minimum size which can be obtained by the photo etching technique.

Next, as shown in Fig. 6P, the polysilicon film 74 is selectively etched by an RIE method, for example, to form a pattern corresponding to the second-layered gate 20 with the photoresist 76 used as a mask. Then, for example, a heat treatment is effected to activate the phosphorus and arsenic ions in the doped regions 56 and 70 in the substrate 10 so as to form n-type short regions 22 and 24.

After this, although not shown in the drawing, an interlayer insulation film is formed, a preset wiring layer is formed and a protection film is formed to complete the mask-ROM manufactured by the manufacturing method according to one embodiment of this invention.

According to the above manufacturing method, the opening 48 formed in the silicon nitride film 36 is substantially equal to the pattern of the first-layered gate 18. The short region 22 for converting the cell transistor of the first-layered gate into the depletion type can be formed in self-alignment with the silicon nitride film 36 having the opening 48. Further, the short region 24 for converting the cell transistor of the second-layered gate into the depletion type can be formed in self-alignment with the pattern of the first-layered gate. As a result, it is

not necessary to provide a mask alignment margin for formation of the short regions 22 and 24.

Therefore, a mask-ROM in which a distance 12 between the first-layered gates is small as shown in Fig. 5 and which is suitable for high integration density can be manufactured. Further, since the distance 12 can be made smaller, it becomes possible to set the gate length L1 of the first-layered gate substantially equal to the second-layered gate length L2.

Next, a case wherein a mask misalignment has occurred at the time of patterning the second-layered gate is explained with reference to Figs. 7A and 7B. Fig. 7A is a cross sectional view showing the case wherein the photoresist is formed in deviated position in the step of Fig. 6O, and Fig. 7B is a cross sectional view of a structure obtained after an etching process is effected for the structure of Fig. 7A. In Figs. 7A and 7B, portions which are the same as those in Figs. 6O and 6P are denoted by the same reference numerals, and only different portions are explained.

Assume that the mask misalignment has occurred in the step of Fig. 6O, for example, and the pattern of the photoresist 76 is formed to partly cover a step portion as shown in Fig. 7A. Then, if the photoresist 76 which partly covers the step portion is used as a mask to selectively etch the polysilicon film 74, a pattern of the second-layered gate 20 shown in Fig. 7B can be obtained.

In such a case, that portion of the polysilicon film 74 which is formed on the step portion is thicker than the remaining portion. Even if the mask for forming the second-layered gates 20 is misaligned but a little, it is only the thicker portion of the film 74 which is etched, never the thinner portion thereof formed between the first-layered gates 18. Hence, no offsets take place in the second-layered gates 20, even if the thicker portion of the film 74 is etched in excess. As a result, the yield of the mask-ROM is not lowered.

According to the invention, it is possible to form the first-layered gates 20 such that they have a width equal to the opening size R7 shown in Fig. 6O. If this is the case, the photoresist 76 overlaps the step portion of the second polysilicon film 74 even if the mask is misaligned, and no offsets occur in the second-layered gates 20.

Moreover, according to the invention, when the pattern size r1 and the opening size R1, both shown in Fig. 6B, are of a minimum value which photolithography can give them, the width of the first-layered gates 18 and the distance between any two adjacent gates 18 are nearly equal to the minimum value. Similarly, when the pattern size r4 and the opening size R7, both shown in Fig. 6O, are of a minimum value that photolithography can give them, the width of the second-layered gates

20 and the distance between any two adjacent first-layered gates 18 are nearly equal to the minimum value. Not only the first-layered gate pattern, but also the second-layered gate pattern can have the minimum size. Hence, the photoresist 76 overlaps the step portion of the second polysilicon film 74 even if the mask is misaligned, and no offsets occur in the second-layered gates 20.

Next, a first modification of the above embodiment is explained with reference to Figs. 8A and 8B.

Fig. 8A is a cross sectional view corresponding to Fig. 6M and Fig. 8B is a cross sectional view corresponding to Fig. 6N.

As shown in Fig. 8A, it is not always necessary to completely remove the silicon oxide film 58 in the above embodiment, and it is possible to leave the silicon oxide film 58 on the first-layered gate 18. Then, the exposed surface of the polysilicon of the first-layered gate 18 is subjected to a thermal oxidation process, for example, to form the silicon oxide film 72. Next, as shown in Fig. 8B, a third-layered polysilicon film 74 which is used for forming second-layered gates is formed on the entire surface of the semiconductor structure.

As described above, the silicon oxide film 58 may be left on the first-layered gate 18.

Next, a second modification is explained.

In the above embodiment, the first-layered gate 18 and second-layered gate 20 are formed of polysilicon, but they can be formed of refractory metal silicide such as molybdenum-silicide or tungsten-silicide. In this case, a silicide film may be formed instead of the first polysilicon film 32 in the step shown in Fig. 6A and a silicide film may be formed instead of the third polysilicon film 74 in the step shown in Fig. 6N. Further, as shown in Fig. 9, each of the first-layered gate 18 and second-layered gate 20 can be formed of a laminated film of a polysilicon film 80 and a silicide film 82. In this case, the polysilicon film 80 is formed instead of the first polysilicon film 32 in the step shown in Fig. 6A and then the silicide film 82 is formed. Further, the polysilicon film 80 may be formed instead of the third polysilicon film 74 in the step shown in Fig. 6N and then the silicide film 82 may be formed.

Fig. 9 is a cross sectional view corresponding to Fig. 4, and portions which are the same as those in Fig. 4 are denoted by the same reference numerals.

### Claims

1. A mask-ROM manufacturing method characterized by comprising:

a step (a) of insulatively forming a first conduc-

tive layer on a semiconductor substrate of a first conductivity type;

a step (b) of forming a first material film which is inactive on said first conductive layer;

5 a step (c) of forming a second material film which is active on said first material film;

a step (d) of patterning said second material film;

a step (e) of increasing the volume of said second material film by altering the material of said second material film patterned;

10 a step (f) of patterning said first material film with said second material film having an increased volume as a mask and forming windows for doping first impurity in said first material film;

a step (g) of selectively doping impurity of a second conductivity type from said first impurity doping window into said substrate through said first conductive layer;

15 a step (h) of selectively altering the material of the surface of said first conductive layer with said patterned first material film used as a mask to selectively form a material altered region on the surface of said first conductive layer;

a step (i) of patterning said first conductive layer with said material altered region used as a mask to form first-layered gates and form second impurity doping windows in said first conductive layer;

20 a step (j) of selectively doping impurity of the second conductivity type from said second impurity doping window into said substrate;

a step (k) of insulatively forming a second conductive layer over said first conductive layer and substrate; and

25 a step (l) of patterning said second conductive layer to form second-layered gates.

2. A manufacturing method according to claim 1, characterized in that said first material film is a difficult-to-oxidize material film.

30 3. A manufacturing method according to claim 2, characterized in that said a difficult-to-oxidized material film is a silicon nitride film.

4. A manufacturing method according to claim 1, characterized in that said second material film is an easily-oxidizable material film.

45 5. A manufacturing method according to claim 4, characterized in that said easily-oxidizable material film is formed of polysilicon.

6. A manufacturing method according to claim 1, characterized in that said step (e) is an oxidizing step.

7. A manufacturing method according to claim 1, characterized in that said first conductive layer is formed of polysilicon.

8. A manufacturing method according to claim 1, characterized in that said first conductive layer is formed of silicide.

9. A manufacturing method according to claim 1, characterized in that said first conductive layer is formed of a laminated structure of films formed of polysilicon and silicide.

10. A manufacturing method according to claim 1, characterized in that said second conductive layer is formed of polysilicon.

11. A manufacturing method according to claim 2, characterized in that said second conductive layer is formed of silicide.

12. A manufacturing method according to claim 1, characterized in that said second conductive layer is formed of a laminated structure of films formed of polysilicon and silicide.

13. A manufacturing method according to claim 1, characterized in that said step (g) is effected by selectively closing said first impurity doping windows with a photoresist and selectively doping impurity of the second conductivity type from the window which is not closed into said substrate through said first conductive layer.

14. A manufacturing method according to claim 1, characterized in that said step (j) is effected by selectively closing said second impurity doping windows with a photoresist and selectively doping impurity of the second conductivity type from the window which is not closed into said substrate.

15. A manufacturing method according to claim 1, characterized in that said step (h) is an oxidizing step.

16. A manufacturing method according to claim 1, characterized by further comprising a step (m) of forming a third material film on said first conductive layer, said step (m) being effected between said steps (a) and (b).

17. A manufacturing method according to claim 16, characterized in that said third material film is a film used for making it easy to remove said first material film from said first conductive layer.

18. A manufacturing method according to claim 16, characterized in that said third material film is a silicon oxide film.

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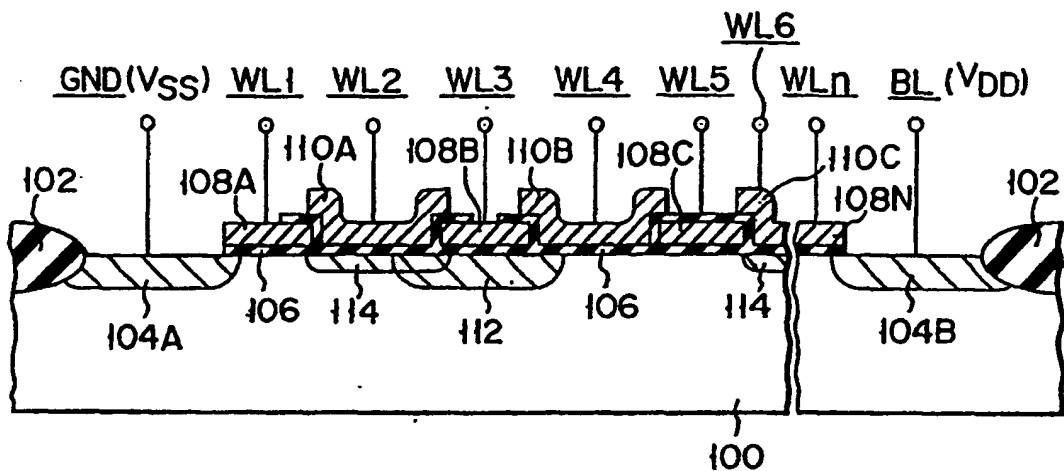
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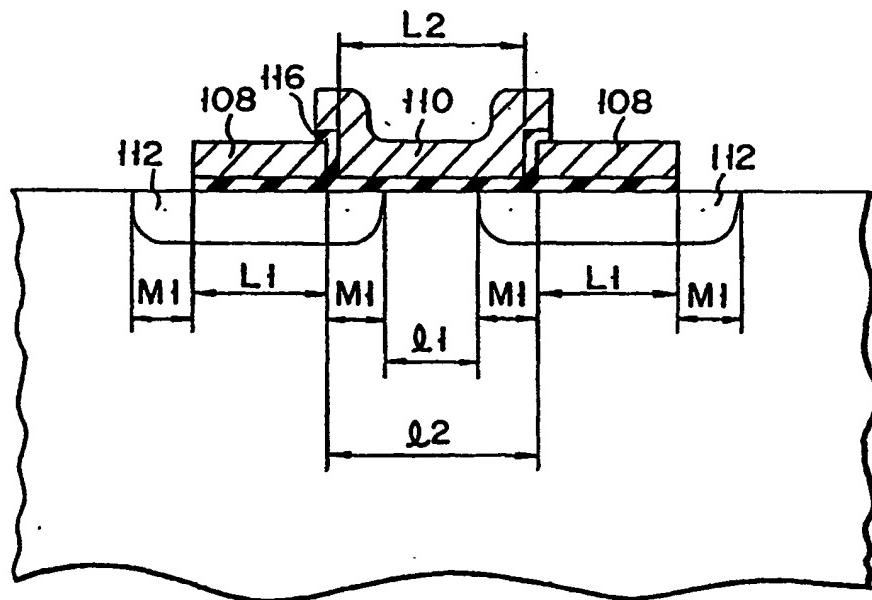
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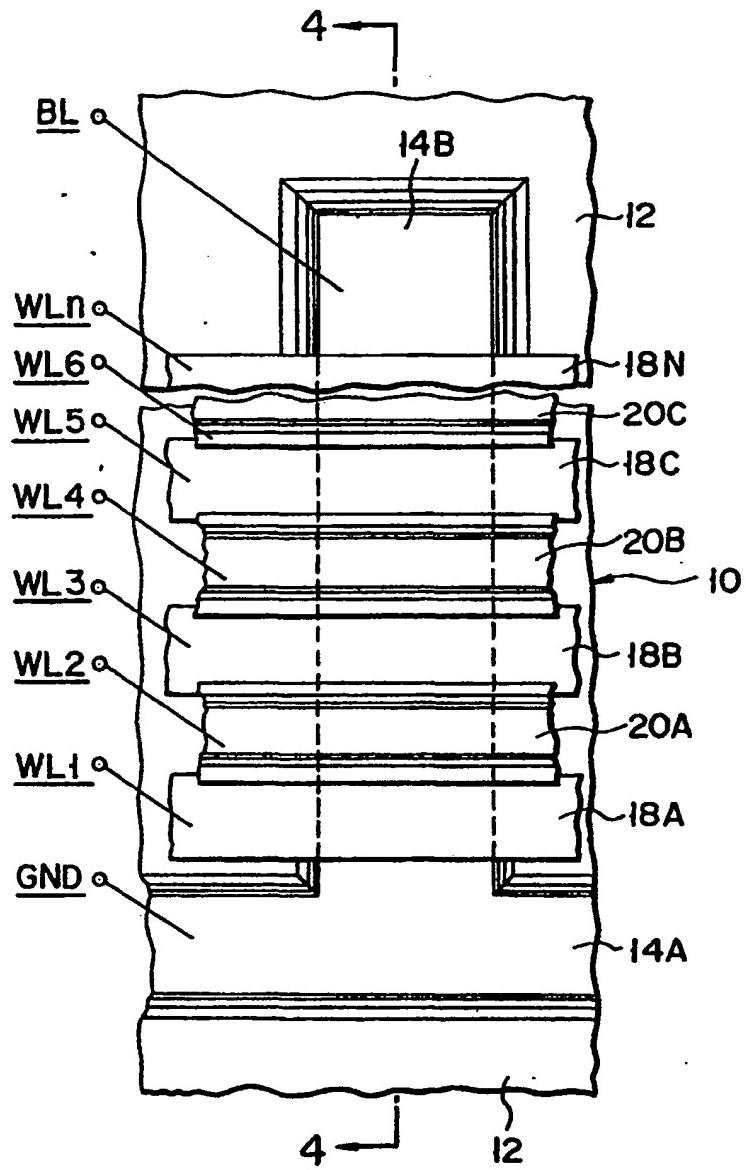
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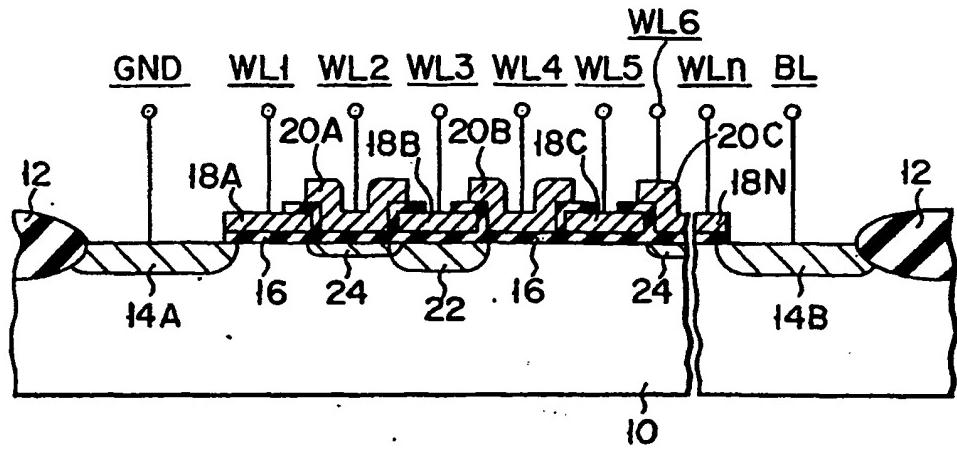
F I G. 1



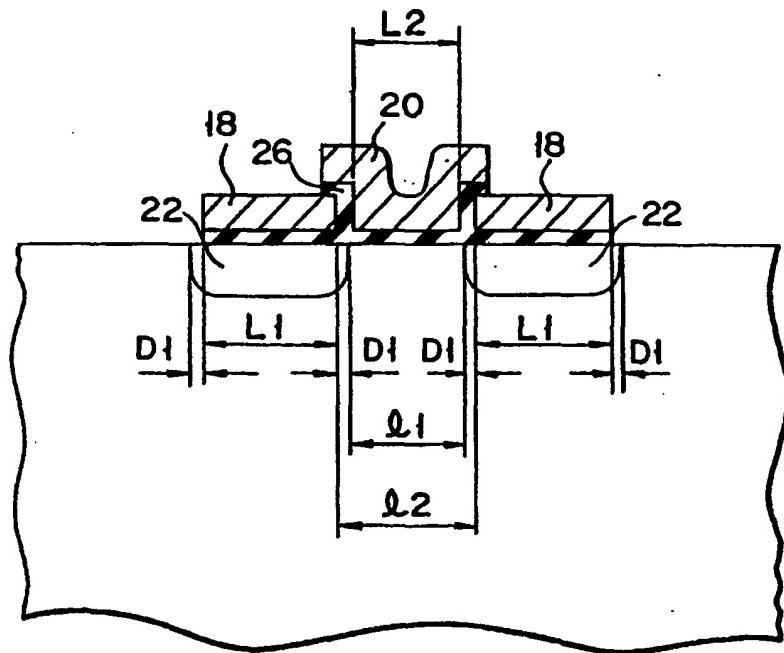
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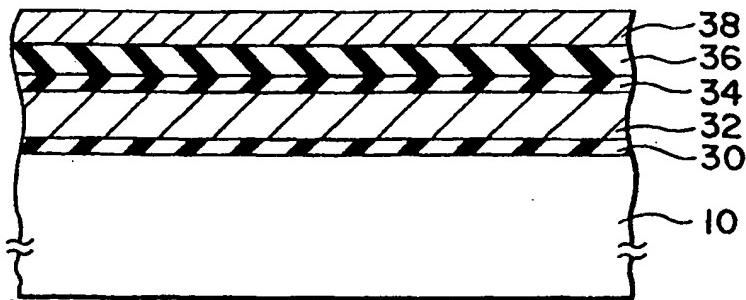
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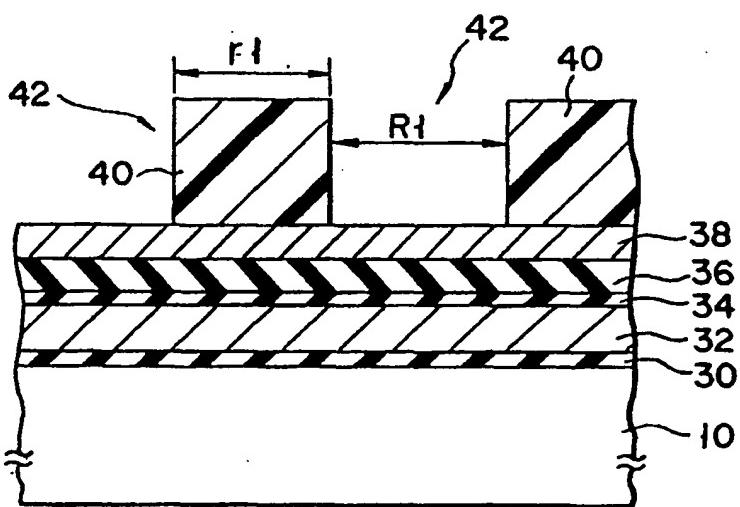
F I G. 4



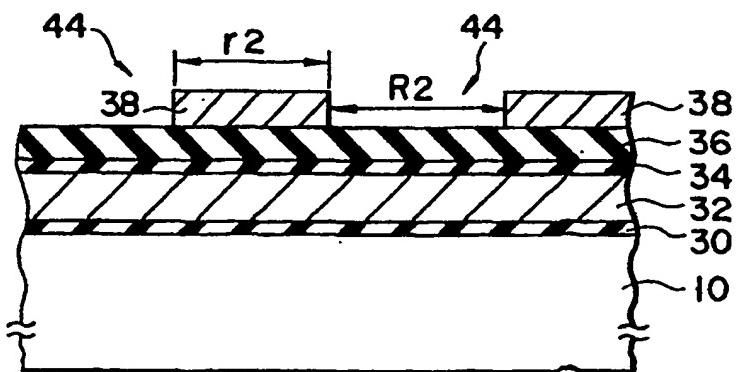
F I G. 5



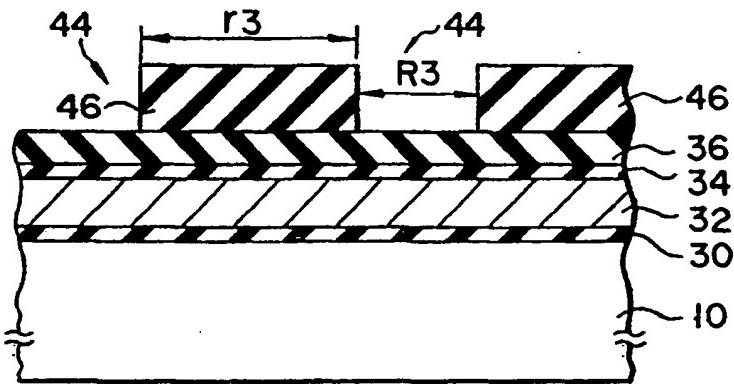
F I G. 6A



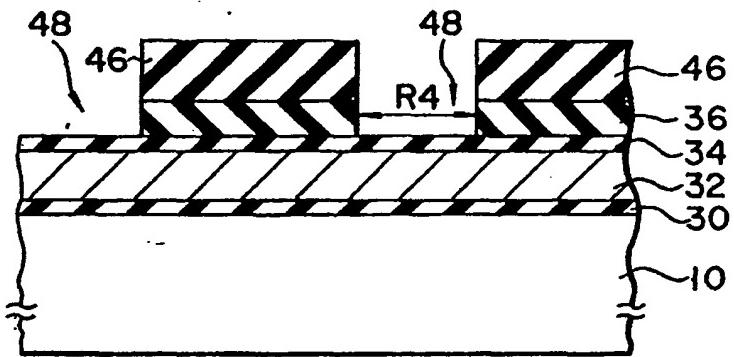
F I G. 6B



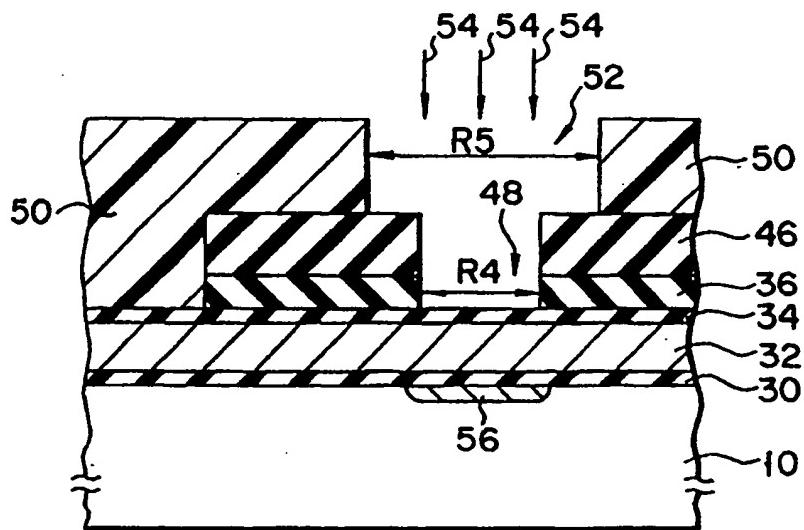
F I G. 6C



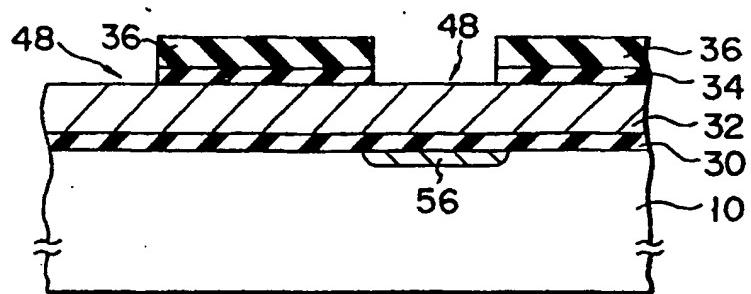
F I G. 6D



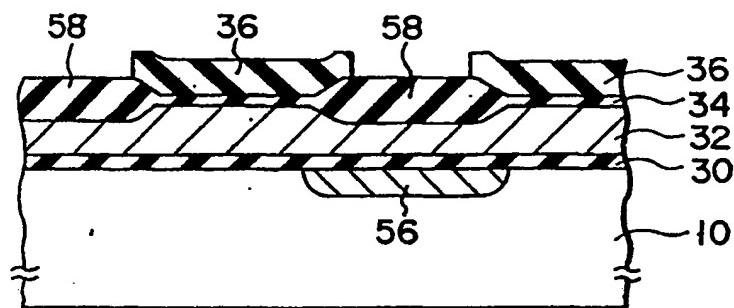
F I G. 6E



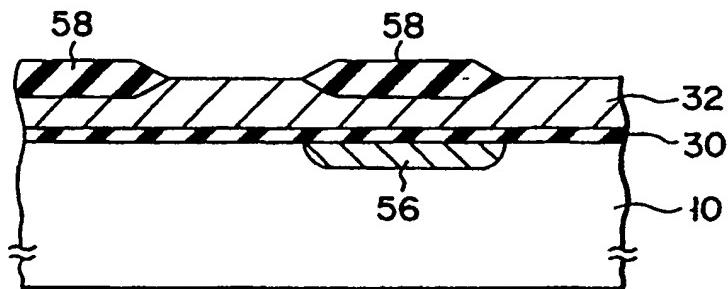
F I G. 6F



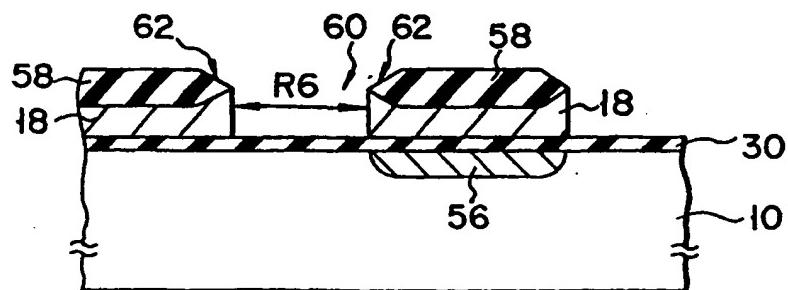
F I G. 6 G



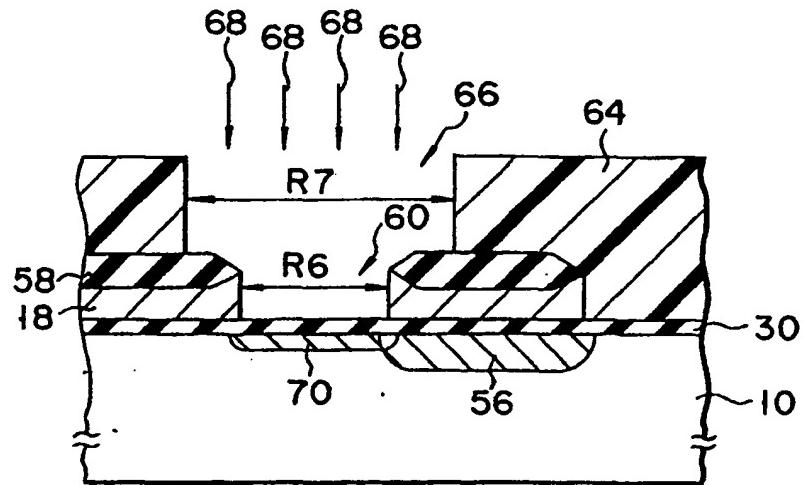
F I G. 6 H



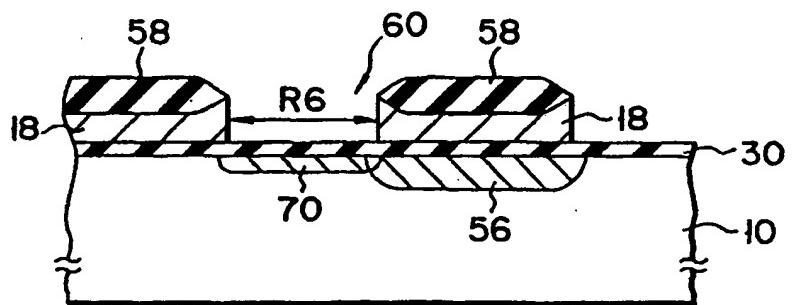
F I G. 6 I



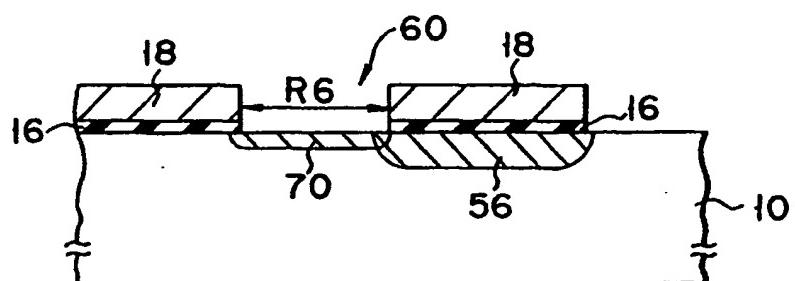
F I G. 6 J



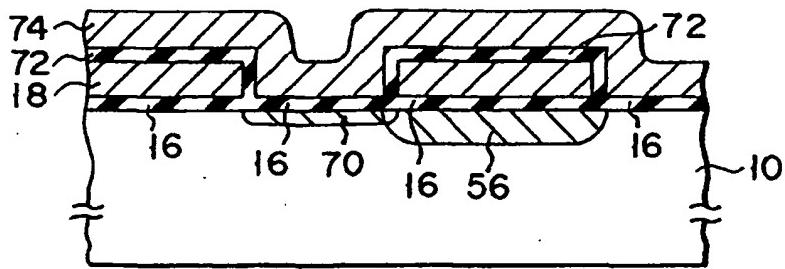
F I G. 6K



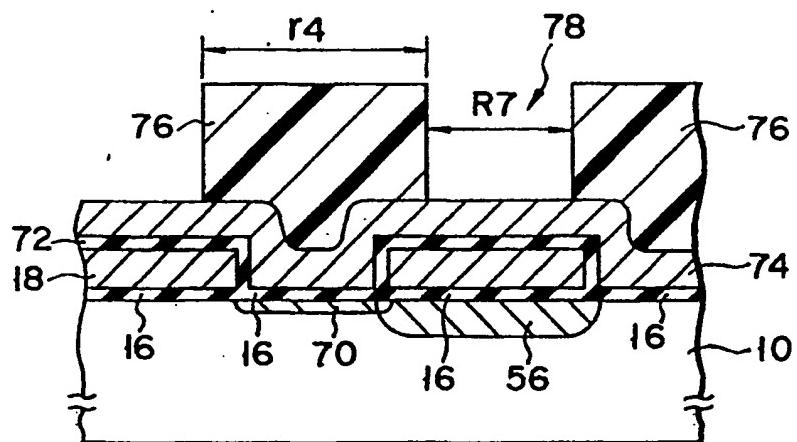
F I G. 6L



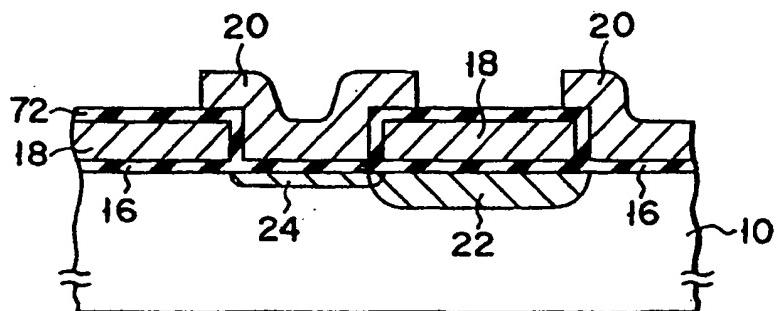
F I G. 6M



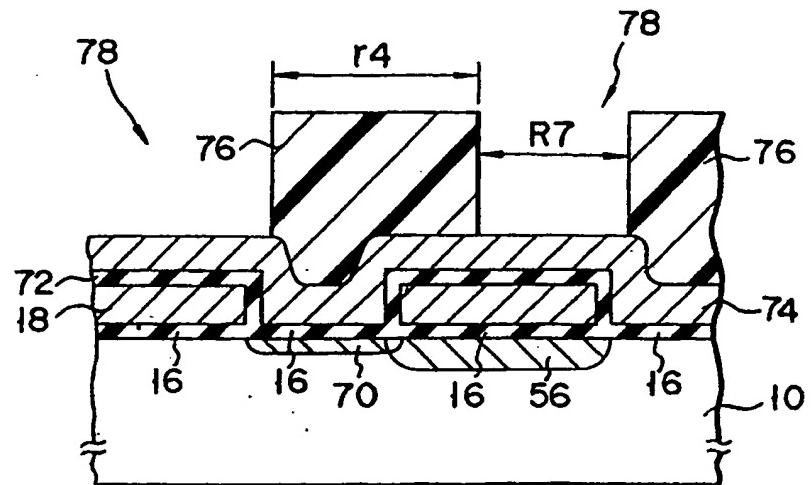
F I G. 6N



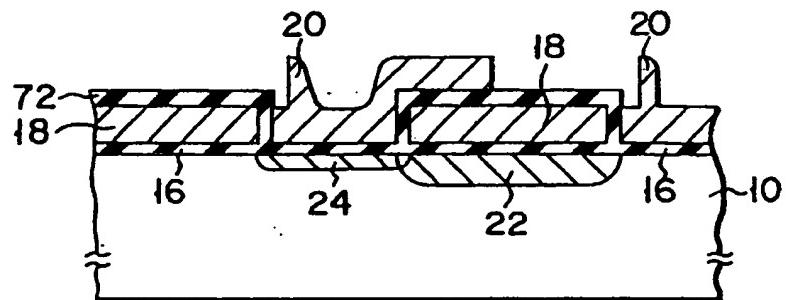
F I G. 6O



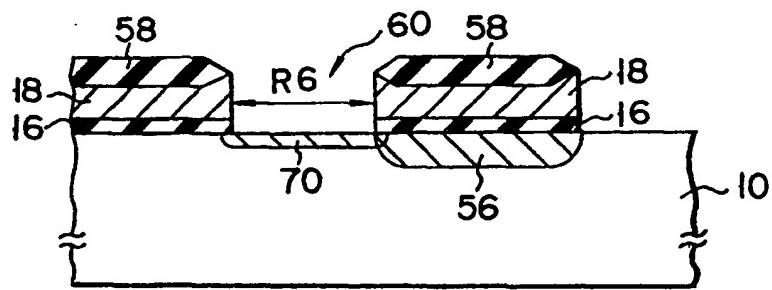
F I G. 6P



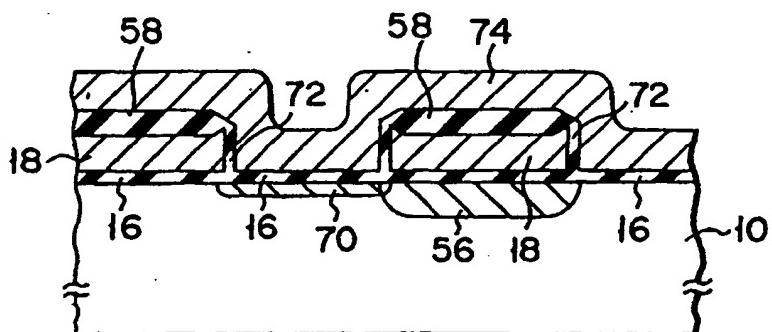
F I G. 7A



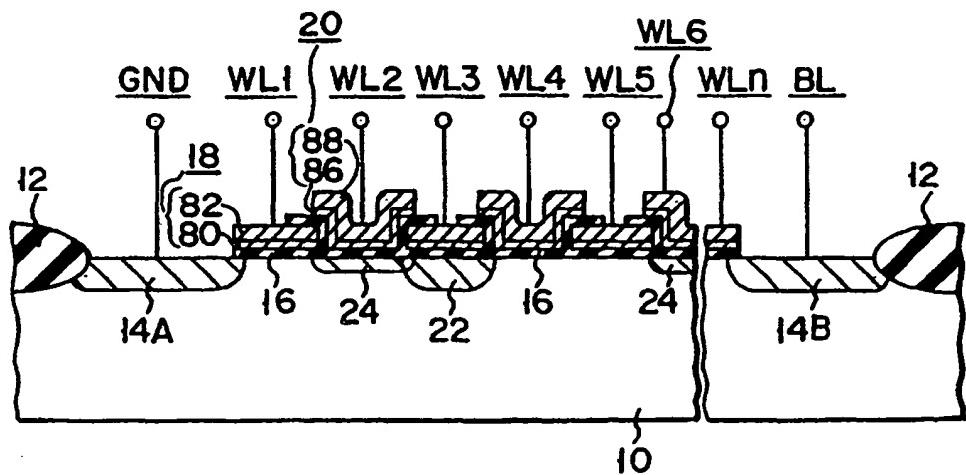
F I G. 7B



F I G. 8A



F I G. 8B



F I G. 9